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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,053	11/18/2003	Bruce G. Hazelzet	BUR920020085US1	1052

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EXAMINER	
TRAN, MICHAEL THANH	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 02/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

EK

Office Action Summary	Application No.	Applicant(s)	
	10/707,053	HAZELZET ET AL.	
	Examiner	Art Unit	
	Michael t. Tran	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *November 18, 2003 through April 19, 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-10 and 13-16* is/are rejected.

7)☒ Claim(s) *5,11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

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PRIMARY EXAMI

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *111803*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the Communications dated November 18, 2003 through April 19, 2004, claims 1-16 are active in this application.

Foreign Priority

2. Our records show that there is no claim of foreign priority.

Information Disclosure Statement

3. The information disclosure statement filed November 18, 2003 has been considered.

Claim Objections

4. Claims 5, 11, 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

It appears that the period, first occurrence of claim 1, should be replaced with a comma.

The DRAMS referred in claim 3, are they the same as the ones referred to in claim 1?

It is unclear which elements the "means for changing modes" belong to. Is it within the memory controller or the memory system? See claim 7.

It is unclear what is being meant by "...to change...", claim 10, line 8.

Claim Rejections – 35 U.S.C. § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

6. Claims 1, 2 and 9 are rejected under 35 U.S.C 102(e) as being anticipated by Wong et al. [U.S. Patent #6,414,868].

With respect to claim 1, Wong et al. disclose, in figures 2, 3 and 5, a memory system comprising: a plurality of DRAMs [1002] having circuits to accept non-inverted input signals [A13, RAS and CAS] and inverted input signals [RAS and CAS via 2003], a register [2000] programmed to provide inverted or non-inverted signals to the DRAMs.

With respect to claim 2, Wong et al. disclose, in figure 5, re-drive circuitry [2001], which can output both non-inverted and inverted polarity signals from one or more input signals. Element 2001 receives non-inverted and inverted signals [A13, RAS and CAS] and outputs the results.

With respect to claim 9, Wong et al. disclose, in figures 2, 3 and 5, that the register drivers either non-inverted or inverted signals to the DRAMs using a programmable pin. It is interpreted that the pins are programmable since they are able to receive the applied signals whenever they are active.

7. Claims 6-8 are rejected under 35 U.S.C 102(e) as being anticipated by Wong et al. [U.S. Patent #6,414,868].

With respect to claim 6, Wong et al. disclose, in figures 2, 3 and 5, a memory system comprising: a plurality of DRAMs [1002] having circuits to accept non-inverted input signals [A13, RAS and CAS] and inverted input signals [RAS and CAS via 2003]; and a memory controller [2000] which can drive either non-inverted or inverted signals to the DRAMs using a programmable pin [see figures]. It is interpreted that the pins are programmable since they are able to receive the applied signals whenever they are active.

With respect to claim 7, Wong et al. disclose, in figures 2, 3 and 5, that the memory system contains a memory controller [2000] and that it is understood that the memory controller "operates" when it is being activated – powerup. As for the memory

for changing modes after powerup, it is understood that a memory system has a mechanism for turning it on and off.

With respect to claim 8, Wong et al. disclose, in figures 3, and 4c, that the pin is hardwired [coupled] to the DRAMs.

8. Claims 10-14 are rejected under 35 U.S.C 102(e) as being anticipated by Wong et al. [U.S. Patent #6,414,868].

With respect to claim 10, Wong et al. disclose, in figures 2, 3 and 5, a memory system comprising: a module having a plurality of DRAMs [1002] with inputs [address inputs] and outputs [for read out data] and circuits [column/row decoders are directly connected to element 2000 which contain inverters for the purpose of "inverting" a particular signal – see figure 5 for inverting structures; and column 1 for DRAM circuitry] to accept either non-inverted input signals [A13, RAS and CAS] and inverted input signals [RAS and CAS via 2003]; a means [pins coupled between 1002 and 2000] connected to the circuits for changing modes to accept inverted input signals; and a memory controller [2000] which is programmable to operate in non-inverted mode at power up [when power is on] and to change after it is programmed [turned off – no power to the device].

With respect to claim 13, Wong et al. disclose, in figures 3 and 4c, that the pin is hardwired [coupled] to the DRAMs.

With respect to claim 14, Wong et al. disclose, in figures 3 and 4c, that the controller 2000 includes pins to convey signals to DRAMs 1002.

9. Claim 15 is rejected under 35 U.S.C 102(e) as being anticipated by Wong et al. [U.S. Patent #6,414,868].

With respect to claim 15, Wong et al. disclose, in figures 2, 3 and 5, a DIMM comprising: a plurality of DRAMs [1002] with means for operating with non-inverted or inverted signals based on a pre-selected operating mode *[column 1, lines 30-50, states that there exists a plurality of circuits [decoders] and that the control circuit [2000] conveys a plurality of inverted and non-inverted signals [RAS, CAS, A13] these signals are operable in the normal mode, such as, accessing a memory data]*; and signal re-drive circuitry [2000] which generates an output in both non-inverted [A13] and inverted polarity signals [RAS and CAS via 2003] from one or more input signals [RAS and CAS]

10. Claim 16 is rejected under 35 U.S.C 102(e) as being anticipated by Wong et al. [U.S. Patent #6,414,868].

With respect to claim 16, Wong et al. disclose, in figures 2, 3 and 5, a computer system with a memory system comprising: memory devices [1002] and re-drive circuitry [2000] external to the said memory devices, said re-drive circuitry having means [pins – see figures] for outputting both non-inverted and inverted polarity signals [A13, RAS and CAS] from one or more input signals [RAS and CAS], and said memory devices designed to operate with non-inverted or inverted signals based on a selected operating mode [accessing a memory data – see column 1, lines 30-55].

Claim Rejections – 35 U.S.C. § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 3 and 4 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Wong et al. [U.S. Patent # 6,414,868] in view of Deml et al. [U.S. Patent # 6,693,483].

With respect to claim 3, Wong et al. Wong et al. disclose, in figures 2, 3 and 5, a memory system comprising: a plurality of DRAMs [1002] having circuits to accept non-inverted input signals [A13, RAS and CAS] and inverted input signals [RAS and CAS via 2003], a register [2000] programmed to provide inverted or non-inverted signals to the DRAMs. Further, Wong et al. also disclose, in figure 3, that the element 2000 contain electrodes connecting to the pins that receive A13, CASO, RASO. It is interpreted that the pins are programmable since they are able to receive the applied signals whenever they are active.

Wong et al. discloses all of the above mentioned but is silent about the fact that the DRAMs operate in either non-inverted or inverted modes. However, column 1, lines 20-35 of Deml et al., shows that it is well known and necessary to have high positive and also negative voltages [non-inverted and inverted modes] applied to DRAMs during

operation. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Wong et al. memory circuit element to include the two above modes as taught by Deml et al., since Deml et al. show that it is well known and desirable in the art to provide a memory circuit element with two modes during operation in order to facilitate data. See column 1, lines 15-35.

With respect to claim 4, Wong et al. disclose, in column 1, lines 45, that the memory is applicable to a DIMM.

Allowable Subject Matter

13. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- Wherein one programmable pin is connected to ground to provide one mode and the other programmable pin is connected to Vdd to operate in the other mode.
- Wherein pre-selected DRAMs may operate in the inverted mode with some critical signals remaining in a non-inverted mode.
- Wherein the memory controller may operate in the inverted mode with some critical signals remaining in non-inverted mode.

Conclusion

14. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited

to assist the Examiner in the prosecution of this case.

15. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

16. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-1650.

Michael T. Tran
Art Unit 2827
February 3, 2006

MICHAEL TRAN
PRIMARY EXAMINER